

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: :
: :
Robert Sheffield et al. : : Group Art Unit: 1753
Appln. No.: 10/667,491 : : Examiner: Luan V. Van
Filed: September 23, 2003 : : Confirmation No. 1242
For: REDUCED CIRCUIT TRACE : :
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PERFORMANCE : :

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Commissioner for Patents
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REQUEST FOR PRE-APPEAL BRIEF CONFERENCE

Pursuant to the Pre-Appeal Brief Conference Pilot Program announced in the Official Gazette, Applicant hereby requests a pre-appeal brief conference in the above-referenced patent application.

The present patent application was filed on September 23, 2003. On September 12, 2005, an initial Office Action was issued requiring election/restriction of/to claims 1-6 or claims 7-18. Applicants traversed this election/restriction requirement, but provisionally elected claims 1-6 as required. On October 19, 2005, an Office Action was issued rejecting claims 1-6 under 35 U.S.C. § 102(b) as either being anticipated by or obvious in view of Taylor et al. (U.S. Patent No. 6,309,528), Ozeki et al. (U.S. Patent Application Publication No. US2002/0060090), Nagai et al. (U.S. Patent Application Publication No. US2002/0155021), and Taylor et al. (U.S. Patent No. 6,558,231). Applicants responded to this Office Action by amending claims 1 and 2, adding claims 19 and 20, and arguing that none of the cited references teach, or even suggest, the claimed invention. Then, on March 8, 2006, an Office Action was issued rejecting claims 1-6, 19, and 20 under 35 U.S.C. § 102(b) as either being anticipated by or obvious in view of Tanaka et al. (U.S. Patent No. 4,959,507), Taylor et al. (U.S. Patent No. 6,309,528), Ozeki et al. (U.S. Patent Application Publication No. US2002/0060090), Nagai et al. (U.S. Patent Application

Publication No. US2002/0155021), Taylor et al. (U.S. Patent No. 6,558,231), and Lin et al. (U.S. Patent No. 5,273,938). Applicants responded to this Office Action by arguing, similar to before, that none of the cited references teach, or even suggest, the claimed invention. Thus, despite repeated attempts to convince the Examiner that the cited references clearly fail to teach, or even suggest, the claimed invention, the Office has maintained its rejection of claims 1-6, 19, and 20, which is certain to be overturned on appeal. Rather than spending further time reiterating the same arguments clearly establishing that the cited references fail to teach, or even suggest, the claimed invention, Applicant has elected to pursue the new pilot program.

As set forth in greater detail in Applicant's responses dated January 19, 2006, and April 27, 2006, the cited references fails to teach, or even suggest, the claimed invention. Specifically, regarding claim 1, the Examiner asserts that Tanaka et al. teaches the claimed invention. Applicants respectfully disagree for several reasons. Specifically, the Examiner implies that Tanaka et al. teaches a method for improving performance of a signal transmitted via a conductive circuit trace of a circuit board as set forth in claim 1. However, as acknowledged by the Examiner, Tanaka et al. teaches a method for forming a bonded ceramic-metal composite substrate. Thus, the teaching of Tanaka et al. clearly differs from the claimed method as set forth in claim 1.

Also, the Examiner asserts that Tanaka et al. teaches reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. However, Tanaka et al. fails to teach, or even suggest, improving the performance of a signal transmitted via a conductive circuit trace by reducing a surface roughness of at least one surface of the conductive circuit trace, as claimed. In contrast, Tanaka et al. teaches polishing a copper circuit sheet so as to improve heat transmissivity between the copper circuit sheet and an electronic component (e.g., see from column 3, line 64, to column 4, line 13). Indeed, Tanaka et al. even teaches that polishing is only required where an electronic component is to be mounted to a copper circuit sheet so as to improve heat transmissivity therebetween, and that polishing is not required where the electronic component is electrically connected to copper circuit sheet, which would be where signals are

transmitted (e.g., see from column 1, line 67, to column 2, line 7; column 3, lines 1-8). Such a teaching by Tanaka et al. is not even analogous to the claimed invention. Thus, since the method taught by Tanaka et al. is totally different and non-analogous to the claimed invention, Applicants respectfully submit that Tanaka et al. fails to teach, or even suggest, the claimed invention.

The Examiner also asserts that both Taylor et al. and Ozeki et al. teach the claimed invention. Specifically, the Examiner also asserts that both Taylor et al. and Ozeki et al. teach methods for electroplating on at least one surface of a conductive circuit trace. However, it is respectfully submitted that neither Taylor et al. nor Ozeki et al. teach providing a layer of a circuit board having a conductive circuit trace on a surface thereof, and reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed. In contrast, Taylor et al. merely discloses a method of depositing metallic conductors onto the surface of circuit boards, wherein conductive metal is deposited to accommodate both small and large features, while Ozeki et al. merely discloses a method for manufacturing a printed circuit board having a shielded transmission line in order to reduce the effects of external noise. Thus, it is respectfully submitted that neither Taylor et al. nor Ozeki et al. teach, or even suggest, providing a layer of a circuit board having a conductive circuit trace on a surface thereof, and reducing a surface roughness of at least one surface of the conductive circuit trace on the surface of the circuit board layer so as to improve performance of a signal transmitted via the conductive circuit trace, as claimed.

At this point it should be noted that if the Examiner is going to rely upon the theory that the claimed invention is inherent in either Tanaka et al., Taylor et al. or Ozeki et al., "the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

In view of the foregoing, it is respectfully submitted that Tanaka et al., Taylor et al., and Ozeki et al. fail to teach, or even suggest, the claimed invention as set forth in claim 1. Thus, is it further respectfully submitted that claim 1 is allowable over Tanaka et al., Taylor et al., and Ozeki et al..

Claims 2-6, 19, and 20 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-6, 19, and 20 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 2 recites reducing the surface roughness by electropolishing the at least one surface, electrochemical polishing the at least one surface, electroplating the at least one surface, or vacuum depositing conductive material on the at least one surface. Tanaka et al. fails to disclose any of these claimed techniques. Also, claims 3-5 recite that the surface roughness of the at least one surface is reduced to no more than 20 microinches root-mean-squared (RMS), 10 microinches root-mean-squared (RMS), or 5 microinches root-mean-squared (RMS). The Examiner asserts that Tanaka et al. teaches such surface roughnesses by disclosing that a surface roughness of no more than 3 μm and no greater than 18 μm . However, 20 microinches translates into .508 μm , 10 microinches translates into .254 μm , and 5 microinches translates into .127 μm . Clearly, the claimed surface roughnesses are well below the 3 μm median surface roughness set by Tanaka et al. Accordingly, Tanaka et al. fails to disclose any of these claimed surface roughnesses. Further, claim 6 recites that the at least one surface of the conductive circuit trace includes a surface parallel and proximal to the surface of the circuit board or a surface perpendicular to the surface of the circuit board. Tanaka et al. fails to disclose polishing either of these claimed surfaces.

In view of the foregoing, it is respectfully submitted that the rejections of claims 1-6, 19, and 20 is in error. Accordingly, for the foregoing reasons, Applicant requests an appeal conference be convened so as to advise Applicant whether the Office will: 1) allow the present claims; 2) reopen prosecution and issue a new office action; or 3) allow this case to proceed to appeal.

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